INTERPOSER FOR IMPEDANCE MATCHING

ABSTRACT

A capacitive interposer (caposer) is disposed inside an integrated circuit package between a die and an inside surface of the package. Conductive layers within the caposer constitute a bypass capacitor. In a through-hole caposer, micro-bumps on the die pass through through-holes in the caposer and contact corresponding landing pads on the package. As they pass through the caposer, power and ground micro-bumps make contact with the plates of the bypass capacitor. In a via caposer, power and ground micro-bumps on the die are coupled to power and ground landing pads on the package as well as to the plates of the bypass capacitor by power and ground vias that extend through the caposer. In signal redistribution caposer, conductors within the caposer redistribute signals between die micro-bumps and package landing pads. In an impedance matching caposer, termination structures within the caposer provide impedance matching to a printed circuit board trace.